

CONDUCTOR ARRANGEMENT FOR REDUCED NOISE DIFFERENTIAL SIGNALLING

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5 ABSTRACT OF THE DISCLOSURE

 A method for analyzing input output (I/O) pin arrangements to determine the effect of differential pair and power and ground pin placement on signal quality which includes constructing an array of pins, arranging a plurality of differential pairs within the array of pins to provide a pin arrangement, exciting each of the differential pairs
10 within the pin arrangement, monitoring coupled noise on other differential pairs within the pin arrangement, and analyzing the pin arrangement based upon the monitoring.